CBCS SCHEME

USN

21EC63

Sixth Semester B.E./B.Tech. Degree Examination, June/July 2025
VLSI Design and Testing

Time: 3 hrs. Max. Marks: 100

Note : *Answer any FIVE full questions, choosing ONE full question from each module.*

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Describe the working of n – type MOSFET with neat diagrams. Derive the equations for drain current. **(10 Marks)**

b. Realize the CMOS gate for the following function :
$Y = \overline{(A+B)C + DE}$. **(03 Marks)**

c. Implement 2 : 1 multiplexes using transmission gate and explain its operation with necessary timing diagram. **(07 Marks)**

OR

2 a. Explain the operation of CMOS inverter with help of transfer characteristics. Explain various region of operation. **(07 Marks)**

b. With necessary circuit diagram operation of tristate inverter, and realize 2 : 1 multiplexer with tristate inverter. **(10 Marks)**

c. Realize 3 i/p NOR gate using CMOS logic. **(03 Marks)**

Module-2

3 a. Explain the steps fabrication of CMOS n – well process with neat sketches. **(10 Marks)**

b. What is λ – based design rules? Write design rules for following layers :
i) Polysilicon ii) Metal iii) n_+ & P_+ diffusion iv) N well. **(06 Marks)**

c. Draw the layout diagram for 2 input NAND Gate. **(04 Marks)**

OR

4 a. Define term "Logical effort". Describe the estimation of logic effort by using example. **(06 Marks)**

b. Estimate parasitic delay of 2 input NAND gate with PMOS width of 2 NMOS width of 2. **(04 Marks)**

c. Draw stick diagram for 3 input NAND gate and estimate the number of tracks and dimensions. **(10 Marks)**

Module-3

5 a. Write the classification of semiconductor memories and explain typical memory organization of RAM memory with neat diagram. **(10 Marks)**

b. Explain operation of full CMOS SRAM cell with necessary topology. **(10 Marks)**

OR

6 a. Differentiate between DRAM and SRAM. **(04 Marks)**

b. Explain the operation of 4 × 4 NOR based ROM array with necessary circuit diagram. **(06 Marks)**

c. Write short notes on :
i) Flash memory cell ii) Ferro electric RAM. **(10 Marks)**

Module-4

7 a. Describe the different types of bridging faults with example. **(06 Marks)**

b. Describe temporary faults in VLSI. **(04 Marks)**

c. For the logic model shown below in Fig. Q7(c), find the Boolean difference with respect to X_2. **(10 Marks)**

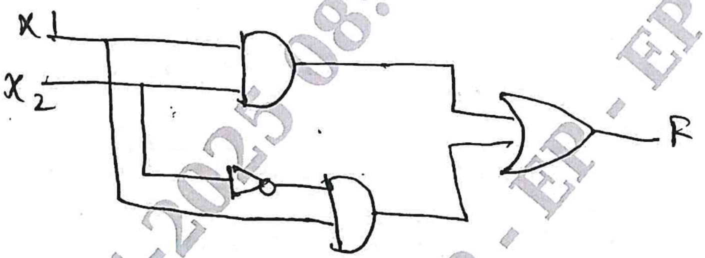

Fig. Q7(c)

OR

8 a. Describe the following term of D algorithm with example.

i) Singular cover ii) Propagation and D – cubes

iii) Primitive D – cubes and fault. **(10 Marks)**

b. What is fault diagnosis? Explain one dimensional path sensitization technique for combinational circuits with an example. **(10 Marks)**

Module-5

9 a. Define following with example :

i) Controllability ii) Observability. **(08 Marks)**

b. Describe any two Adhoc design rules for improving testability. **(06 Marks)**

c. For state table – 1 , find i) Homing sequence ii) Distinguish sequence and iii) Response of machine in homing sequence. **(06 Marks)**

	I/P	
P - state	X = 0	X = 1
A	B . 0	D . 0
B	A . 0	B . 0
C	D . 1	A . 0
D	D . 1	C . 0

OR

10 a. List LSSD design rules. **(10 Marks)**

b. Explain list generation based on functional fault models. **(10 Marks)**

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